MDG-MMS group
Stage proposals on STM32 microcontrollers

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Memories

- Serial EEPROM
- RF memories

Secure MCUs

- Personnal /embedded security
- Secure Hardware platfoms and turnkey solutions

Microcontrollers

- General Purpose 8bit & 32bit MCUs
- Automotive 8-bit MCUs,

Key enablers

State of the art embedded NVM
Advance 8 and 32-bit CPU platforms
System and security expertise
Market leadership in key products

Supporting ST target markets

Automotive | Healthcare | Industrial/Smartgrid | Security | Consumer

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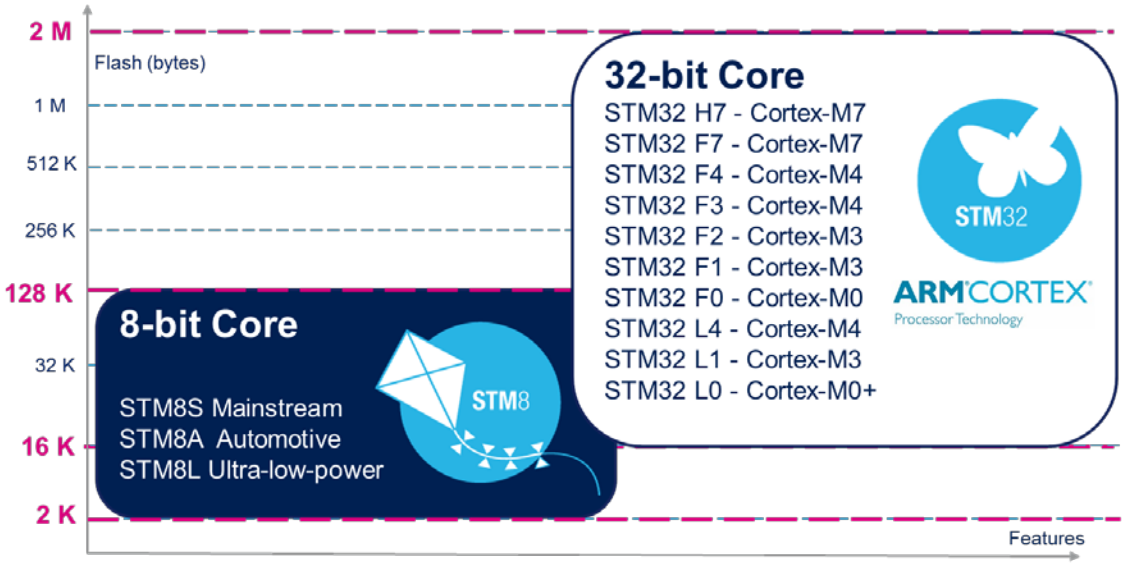
General Purpose MCUs

A Wide range of Product sales Types embedding a rich set of Digital & Analog Peripherals
Enabling selection flexibility on Embedded Flash size as well as performances

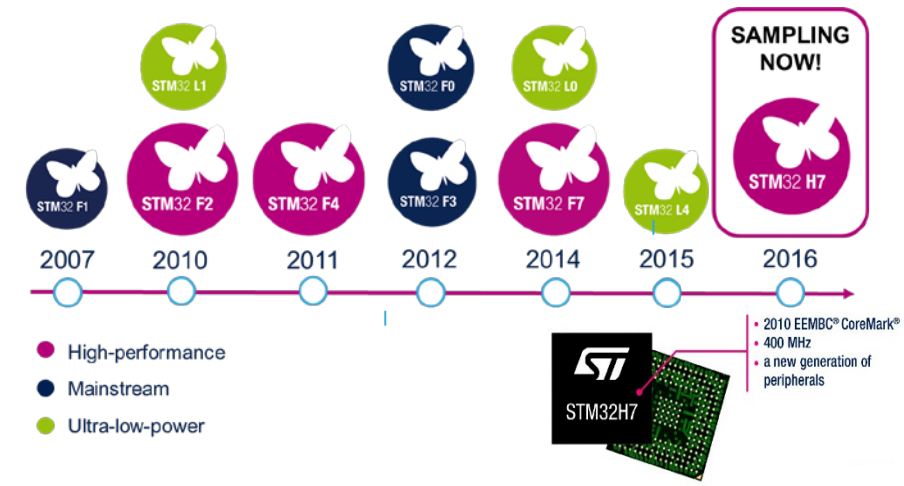


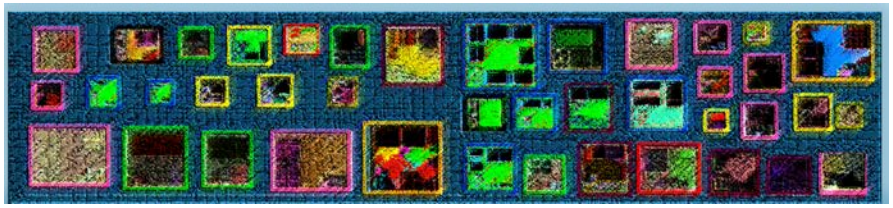
Real-time performance	Outstanding power efficiency	Reach Set of peripherals	Maximum integration
STM32 Dynamic Efficiency ™, ART Accelerator™, Chrom-ART Accelerator™, CCM-SRAM, L1-Cache Multi-AHB bus matrix, Excellent real-time Zero-wait state execution performance from Flash	Dynamic Power 40 – 150 uA/Mhz Stop down to < 1 uA Stand By down to < 300 nA Shutdown downto < 20 nA	USB-OTG High speed, Ethernet, CAN, DFSDM, HR timer, LCD-TFT controller, SRAM interface, crypto/hash processor, true RNG*, PGA, 16-bit ∑Δ ADC and 12-bit ADC (up to 5 MSPS), external memory interface, CEC, SAI	Reset circuitry; voltage regulator, internal RC oscillator, PLL, WLCSP packages

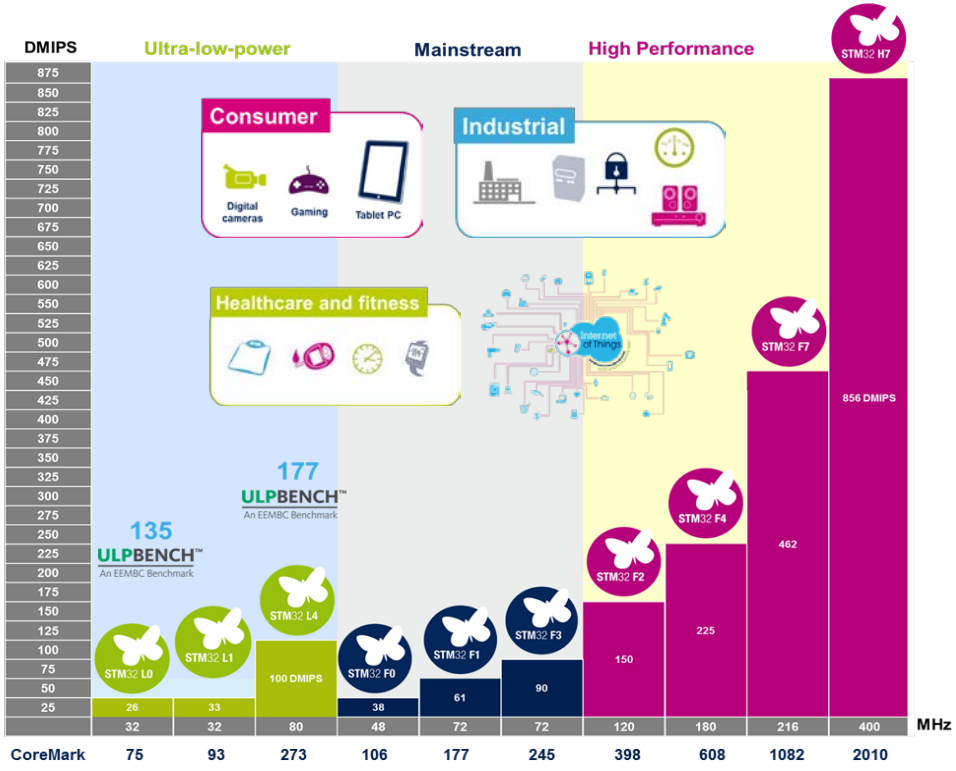
Over 4 Billion Devices Delivered to Broad Range of Markets

STM32 ARM Cortex-M Based MCUs

Keep Innovating! : Highest CoreMark Result on ARM Cortex-M







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STM32 MCU Design Challenges

PRIORITIES

High Performance	Ultra Low Power	Main Stream
Performance:> 800 DMIPS	Dynamic Power efficiency	Dynamic Power Efficiency
Dynamic Power efficiency	Static Power efficiency	Ratio Performance/Power
Static Power efficiency	Performance: > 100 DMIPS	Die Size
Die size	Die size	Static Power Efficiency

CHALLENGES

1. **Power, Robustness, Size Co-Optimization**
   - Multi-VT / Multi-site / Multi-voltage / Multi Process scenarios
   - Ultra low power clock tree
   - EMC , Robustness, Safety Compliancy
2. **Multi-Voltage Design Complexity**
   - Fragmented voltage area hierarchically/topologically
   - Voltage scaling
   - Always On Cells (isolated / not isolated)
3. **System Performances & ARM Cortex-M Cores integration Objectives**
   - Realizing maximum system performance
   - Achieving ultra-low power

Broad diversity of challenges, very aggressive time schedules

Stage Proposals

- 1. Architectural Analysis & Definition of Real Time Safety Diagnostic Hardware for non Automotive Microcontrollers
  - Overview on STM32 microcontrollers
  - Fault Injection simulations on STM32 microcontrollers
  - HW/SW codesign
  - RTL implementation & simulations
- 2. Innovative measurement methodologies on High End STM32 Analog IP peripherals
  - Overview on STM32 analog subsystem
  - Automatic bench measurement design (sw assisted)
  - High End STM32 Analog IPs validation & debug